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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/675,744 | DODSON ET AL. | |
| | Examiner | Art Unit | |
| | Ryan Dare | 2186 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *09/30/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) *8, 10, 16, and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities:

Paragraph 11, line 5 recites the phrase "not need." The examiner believes this should be replaced with the phrase "not needed."

Paragraph 38, line 8 recites the term "ache." The examiner believes this should be replaced with the term "cache."

Appropriate correction is required. It is the duty of Applicant to ensure that the entire specification is free of all minor errors such as those listed above.

### *Claim Objections*

2. Claims 8 and 16 are objected to because of the following informalities: They recite the phrase "snooping a read requests." The examiner believes this should be replaced with "snooping a read request." Appropriate correction is required.

3. Claim 10 is objected to because of the following informalities: It recites "an controller." The examiner believes this should be replaced with "a controller." Appropriate correction is required.

4. Claim 22 is objected to because of the following informalities: It recites "the data is a most coherency copy of the data." The examiner believes this should be replaced with "the data is a most coherent copy of the data." Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 22 is rejected under 35 U.S.C. 102(b) as being anticipated by Arimilli et al., US Patent 5,943,684, hereafter Arimilli '84.

7. Arimilli '84 teach a data processing system, comprising:

an interconnect including an address bus and a data bus, in fig. 1, bus 16;

a plurality of devices interconnected via coupled to said interconnect, in fig. 1, processing unit 11a;

a plurality of caches that are each associated with a device among said plurality of devices, in fig. 1, numeral 15, wherein a first cache associated with a first device includes:

a cache line of a cache having a coherency indicator and coherency mechanism that supports at least a first coherency state, a second coherency state and a third coherency state, wherein:

said first coherency state indicates that data within said first cache line is currently invalid but may or not be overwritten by said first device, in the Upstream undefined state of fig. 3 and described in col. 6, lines 40-43;

said second coherency state indicates that the data is invalid, in the Invalid state of fig. 3;

said third coherency state indicates that the data is a most coherent copy of the data across the plurality of caches, in the Modified state of fig. 3;

means for said first device to issue an address operation requesting sole access to said cache line that the first device intends to overwrite in the first cache in fig. 1, bus 16.

means for changing a coherency state when a response is received indicating that sole ownership has been granted to said first device, in the arrow that transitions to the U state in fig. 3.

### *Claim Rejections - 35 USC § 103*

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1- 2, 7 and 9-11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '84 and Arimilli et al., US Patent Application Publication 2003/0097529, hereafter Arimilli '29.

11. With respect to claim 1, Arimilli '84 teach: In a data processing system having a coherent memory hierarchy that includes a memory and a plurality of caches each assigned to particular ones of a plurality of devices that generate cache access operations, a method of maintaining cache coherency comprising:

a first device issuing an address operation requesting sole ownership of a cache line that said first device intends to overwrite in a first cache, in col. 7, lines 23-34;

changing a coherency state of the cache line within said first cache to a first coherency state that indicates that the first device has sole ownership of the cache line and may or may not overwrite the cache line, in col. 6, lines 40-42;

Arimilli '84 teaches the above limitations, but fails to teach the other limitations of the claim. Arimilli '29 teaches:

in response to snooping said address operation, changing a coherency state of the cache line in a second cache associated with a snooping device to a second state without sending data from said cache line in the second cache to the first cache, in par. 29, lines 1-4;

wherein sole ownership of said cache line is provided to said first device without data being sourced to said first cache from another cache, in the last 6 lines of par. 29;

12. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made,

to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

13. With respect to claim 2, Arimilli '29 teaches the method of Claim 1, wherein, when said first device subsequently initiates a write of said cache line, said method further comprises changing said first state to a third state indicating that a most coherent copy of said data exists within the cache line of the first cache, in the last 5 lines of par. 27.

14. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made, to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

15. With respect to claim 7, Arimilli '29 teaches the method of claim 2, further comprising:

snooping requests for access to said cache line at said first cache, in par. 20;

and when the cache line in the first cache is still in the first coherency state, retrying all snooped requests, wherein all subsequent requests snooped while said cache line is in the first coherency state is retried until the coherency state changes, in par. 20.

16. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made,

to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

17. With respect to claim 9, Arimilli '29 teaches the method of claim 1, wherein said first device is an I/O device and said first cache is an I/O cache controlled by an I/O controller, in par. 18, said method further comprising:

issuing the address operation as a direct memory access (DMA) Claim in response to a speculative DMA write, in par. 18.

18. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made, to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

19. With respect to claim 10, Arimilli '84 teaches the method of claim 1, wherein said first device is a processor and said first cache is a processor cache controlled by a cache controller, in fig. 1, said method further comprising:

issuing the address operation in response to a data cache block zero (DCBZ) operation, in col.7, lines 23-34.

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made, to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol

of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

21. With respect to claim 11, Arimilli '84 teaches:

In a data processing system having a memory hierarchy that includes a memory and a plurality of caches interconnected by a system bus and each accessible by particular ones of a plurality of devices, in fig. 1, a caching mechanism that provides address coherency operations for cache line writes by a first device, said caching mechanism comprising:

a first cache line that has a corresponding cache line in a second cache associated with a second device, in col. 6, lines 41-43;

a coherency tracking mechanism that supports at least a first coherency state, a second coherency state and a third coherency state, wherein:

said first coherency state indicates that data within said first cache line is currently invalid but may or may not be overwritten by said first device, in the Upstream undefined state of fig. 3 and described in col. 6, lines 40-43;

said second coherency state indicates that the data is invalid, in the Invalid state of fig. 3; and

said third coherency state indicates that the data is a most coherent copy of said data, in the Modified state of fig. 3;

means for a first device to issue an address operation requesting sole access to said cache line that said first device intends to overwrite in a first cache, in fig. 1, bus 16;

means for changing a coherency state of said cache line within said first cache to said first coherency state when a response is received on said system bus indicating that sole ownership has been granted to said first cache, in the arrow that transitions to the U state in fig. 3.

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made, to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

23. With respect to claim 20, Arimilli '29 teaches the caching mechanism of claim 1, wherein said first device is an I/O device and said caching mechanism includes an I/O cache controlled by an I/O controller, in par. 18, said method further comprising:

means issuing the address operation as a direct memory access (DMA) Claim in response to a speculative DMA write, in par. 18.

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84 and Arimilli '29 before him at the time the invention was made, to modify the cache coherency protocol of Arimilli '84 with the cache coherency protocol of Arimilli '29 in order to improve processing efficiency and to reduce congestion of the system bus, thereby improving performance, as taught by Arimilli '29 in par. 25.

25. Claims 6, 8, 12-16, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '84 and Arimilli '29 as applied to claims 1- 2, 7 and 9-11, 20

and 22 above, and further in view of Chang, US Patent Application Publication 2003/0115423.

26. With respect to claim 6, Arimilli teaches all other limitations of the parent claims as discussed supra, but fails to teach the snooping method of claim 6. Chang teaches the method of claim 2, further comprising:

snooping requests for access to said cache line at said first cache, in par, 64, lines 7-8.

when the cache line in said first cache is in the third coherency state and said first device has completed writing data to said first cache, sourcing the data from the first cache to the second cache, in par. 65, lines 22-25.

when the cache line in said first cache is in the invalid coherency state, sourcing the data from memory, in par. 68.

27. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

28. With respect to claim 8, Arimilli teaches all other limitations of the parent claims as discussed supra, but fails to teach the snooping method of claim 8. Chang teaches the method of claim 2, further comprising:

snooping a read request for said cache line at said first cache, in par. 64, lines 7-8

when the read request receives a null response and said cache line in the first cache is still in the first coherency state:

sourcing data for the cache line from memory, in par. 68;

changing said first coherency state to an invalid state in said first cache, in fig. 3, the read and invalidate column.

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

30. With respect to claim 12, Arimilli teaches all other limitations of the parent claim as discussed supra, but fails to teach the snooping method of claim 12. Chang teaches the cache mechanism of claim 11, further comprising:

means for snooping the address operation, in par. 64, lines 7-8.

means, when the address operation is snooped while the cache line is in said third coherency state within the snooping device's cache and the snooped operation is for access that does not overwrite the entire cache line, for:

issuing data from the snooping device's cache line on the data bus when said access is granted to said first device, in par. 65; and

Arimilli '84 teaches:

changing the coherency state of the snooping device's cache line to another state that indicates that the first device's cache line has data in a

coherency state that is as coherent or more coherent than said snooping device's cache line, in par. 27; and

Chang teaches:

means, when the snooped request is received while the snooping device's cache line is in said third coherency state and the snooped operation is for sole ownership of the cache line that is to be completely overwritten by the first device, for changing a coherency state of the snooping device's cache line to said second state, and withholding any transfer of data to the first device's cache line, in par. 65.

31. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

32. With respect to claim 13, Arimilli '29 teaches the caching mechanism of claim 12, further comprising:

means for overwriting the data within said first device's cache line with data from the first device, wherein said overwriting the data within said first device's cache line with data from the first device, wherein said overwriting is only initiated after sole ownership has been granted and said first cache line is in said first coherency state, in the last 6 lines of par. 29; and

subsequently changing the coherency state of the first device's cache line to the third state indicating that a most coherent copy of said data exists within the first device's cache line, in the last 5 lines of par. 27.

33. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

34. With respect to claim 14, all other limitations of the parent claims are taught as discussed supra. Furthermore, Chang teaches the caching mechanism of claim 13, further comprising:

means for snooping requests for access to said cache line from a requesting device, in fig. 1, interconnect 108;

means, when the cache line is in the third coherency state and said first device has completed writing data to said cache line, for sourcing the data from the cache line to the requesting device, in fig. 1, interconnect 108 which connects all the devices;

means, when the cache line is in the second coherency state, for indicating that said data should be sourced from memory, in par. 65.

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency

protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

36. With respect to claim 15, all other limitations of the parent claims are taught as discussed supra. Furthermore, Arimilli '29 teaches the caching mechanism of claim 13, further comprising:

means for snooping requests for access to said cache line at said first cache, in system bus 157 of fig. 1B ,and described in par. 20;

means, when the first device's cache line is still in the first coherency state, for retrying all snooped requests, wherein all subsequent requests snooped while said cache line is in the first coherency state is retried until the coherency state changes, in fig. 1, system bus 157, and described in par. 20.

37. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

38. With respect to claim 16, all other limitations of the parent claims are taught as discussed supra. Furthermore, Chang teaches the caching mechanism of claim 13, further comprising:

means for snooping a read request for said cache line at said first cache, fig. 1, interconnect 108 and described in par. 64, lines 7-8

means, when the read request receives a null response and said cache line in the first cache is still in the first coherency state, for:

indicating that data for the cache line should be sourced from memory, in fig. 1 and described in par. 68; and

changing said first coherency state to an invalid state in said first cache, in fig. 3, the read and invalidate column.

39. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

40. With respect to claim 23, Arimilli '84 teaches the limitations of the parent claims as discussed supra. Chang teaches the data processing system of claim 22, further comprising:

means for a snooping device to snoop the address operation, in par. 64, lines 7-8.

means, when the snooping device snoops the address operation while the snooping device's cache line is in said third coherency state and the snooped operation is for access that does not overwrite the entire cache line, for:

issuing data from the snooping device's cache line on the data bus when said access is granted to said first device, in par. 65; and

Arimilli '84 teaches:

changing the coherency state of the snooping device's cache line to another state that indicates that the first device's cache line has data in a coherency state that is as coherent or more coherent than said snooping device's cache line, in par. 27; and

Chang teaches:

means, when the snooped request is received while the snooping device's cache line is in said third coherency state and the snooped operation is for sole ownership of the cache line that is to be completely overwritten by the first device, for changing a coherency state of the snooping device's cache line to said second state, and withholding any transfer of data to the first device's cache line, in par. 65.

means, when the snooped operation is received, for changing the coherency state of the cache line in the first cache to the first coherency state when sole access granted to the first device's cache, in the Exclusive Respond state as described in par. 65.

41. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli '84, Arimilli '29 and Chang before him at the time the invention was made, to modify the cache coherency protocol of Arimilli with the cache coherency protocol of Chang, in order to limit main-memory accesses, which avoids bottlenecks, as taught by Chang in par. 9.

42. Claims 3-5 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli '84, Arimilli '29 and Chang as applied to claims 1-2, 6-16, and 20-23 above,

and further in view of Chaudhry, et al., US Patent Application Publication 2002/0199063.

43. With respect to claim 3, all other limitations of the parent claims are taught as discussed supra, but fail to teach speculatively issuing operations. Chaudhry et al. teach the method of claim 1, wherein said address operation for sole ownership of a cache line is generated for a speculatively issued cache line overwrite operation, said method further comprising:

speculatively issuing the address operation for sole ownership of the cache line, in par. 14; and

determining whether said cache line overwrite operation was correctly speculated, wherein said first coherency state is changed to another coherency state depending on whether said cache line overwrite operation was correctly speculated, in par. 142.

44. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli, Chang and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chang with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

45. With respect to claim 4, all other limitations of the parent claims are taught as discussed supra. Chaudhry et al. teach the method of claim 3, wherein when said cache line overwrite operation was not correctly speculated, said method further comprises:

changing the coherency state of the cache line in the first cache from said first coherency state to an invalid state, in par. 14; and

subsequently sourcing requests for said cache line from memory, in par. 14.

46. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli, Chang and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chang with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

47. With respect to claim 5, all other limitations of the parent claims are taught as discussed supra. Chaudhry et al. teach the method of claim 3, wherein when said cache line overwrite operation was correctly speculated, said method further comprises:

initiating a write of said cache line with data provided by said first device, in par. 142.

changing said first state to a third state indicating that a most coherent copy of said data exists within the cache line of the first cache, in par. 142.

48. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli, Chang and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chang with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

49. With respect to claim 17, all other limitations of the parent claims are taught as discussed supra, but fail to teach speculatively issuing operations. Chaudhry et al.

teach the caching mechanism of claim 11, wherein said address operation for sole ownership of a cache line is generated for a speculatively issued cache line overwrite operation, said system further comprising:

means for speculatively issuing the address operation for sole ownership of the cache line, in par. 14; and

means for determining whether said cache line overwrite operation was correctly speculated, wherein said first coherency state is changed to another coherency state depending on whether said cache line overwrite operation was correctly speculated, in par. 142.

50. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli, Chang and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chang with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

51. With respect to claim 18, all other limitations of the parent claims are taught as discussed supra. Chaudhry et al. teach the caching mechanism of claim 17, wherein when said cache line overwrite operation was not correctly speculated, said mechanism further comprises:

means changing the coherency state of the cache line in the first cache from said first coherency state to an invalid state, in par. 14; and

means for subsequently sourcing requests for said cache line from memory, in par. 14.

52. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli, Chang and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chang with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

53. With respect to claim 19, all other limitations of the parent claims are taught as discussed supra. Chaudhry et al. teach the caching method of claim 17, wherein when said cache line overwrite operation was correctly speculated, said method further comprises:

means for initiating a write of said cache line with data provided by said first device, in par. 142.

means changing said first state to a third state indicating that a most coherent copy of said data exists within the cache line of the first cache, in par. 142.

54. It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli, Chang and Chaudhry before him at the time the invention was made, to modify the cache coherency protocol of Arimilli and Chang with the cache coherency protocol of Chaudhry in order to increase performance by allowing load and instructions to issue speculatively, as taught by Chaudhry in par. 11.

***Conclusion***

55. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to

consider these references fully when responding to this action. The documents cited therein teach similar cache coherency protocols.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Dare
November 9, 2005

MATTHEW D. ANDERSON
PRIMARY EXAMINER